Abstract:

An improved bridge circuit for connecting a disk drive with an ATA interface to a computer via a USB bus. After the bridge receives the first data from the ATA interface, the bridge makes the assumption that the next read command

5   will probably be for the next sequential data word and the interface issues a read command for the next sequential data word. After an accessing delay, the second data word is received by the bridge. When the bridge does in fact receive the next read command from the host, a check is made to see if the second read command is for the next sequential location from the first read

10   command. If it is, the already fetched data is provided to the host without delay. If it is not, the process is handled as was the first read command.